Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (1/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 0756-2131

First Inventor or Application Identifier: Shunpei YAMAZAKI et al.

Title: A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification — *Total Pages* [38]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) — *Total Sheets* [6]
4. [X] Oath or Declaration — *Total Pages* [2]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
   (when there is an assignee)
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. [ ] *Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s)
    (if foreign priority is claimed)
16. [X] Other: Notice of Change of Address

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. **If a CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
Divisional of prior application Serial No. 08/784,294, filed January 16, 1997.
Prior application information: Examiner: F. Abraham Group/Art Unit: 2811

18. CORRESPONDENCE ADDRESS

[X] Customer Number or Bar Code Label — Customer No. 22204 — or [X] Correspondence address below

(Insert Customer No. or Attach bar code label here)

Name: Eric J. Robinson
Firm: NIXON PEABODY LLP
Address: 8180 Greensboro Drive, Suite 800
City: McLean State: VA Zip Code: 22102
Country: U.S.A. Telephone (703) 790-9110 FAX (703) 883-0370

Name: Eric J. Robinson Registration No. 38,285

Signature Date: March 24, 2000

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

 Docket: 0756-2131

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of)
Shunpei YAMAZAKI et al.)
Based On Serial No. 08/784,294) Art Unit: 2811
Which Was Filed: January 16, 1997) Examiner: F. Abraham
For: A METHOD OF MANUFACTURING)
A SEMICONDUCTOR DEVICE) Date: March 24, 2000

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231
Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:

Before the first sentence of the specification, insert --This application is a Divisional of Application Serial No. 08/784,294 filed January 16, 1997.--

REMARKS

This application has been amended to include the continuing application

data thereof.

Examination on the merits is requested.

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an arrangement of a thin film semiconductor device using a crystal silicon film and to a fabrication method thereof.

2. Description of Related Art

Hitherto, there has been known a thin film transistor using a silicon film, i.e. a technology for forming the thin film transistor by using the silicon film formed on a glass substrate or quartz substrate.

The glass substrate or quartz substrate is used because the thin film transistor is used for an active matrix type liquid crystal display. While a thin film transistor has been formed by using an amorphous silicon film in the past, it is being tried to fabricate the thin film transistor by utilizing a silicon film having a crystallinity (referred to as "crystal silicon film" hereinbelow) in order to enhance its performance.

The thin film transistor using the crystal silicon film allows to operate at higher speed by more than two digits as compared to one using the amorphous silicon film. Therefore, peripheral driving circuits of an active matrix type liquid crystal display which have been composed of external IC circuits may be built on the glass substrate or quartz substrate in the same manner with the active matrix circuit.

Such structure is very advantageous in miniaturizing the whole apparatus and in

simplifying the fabrication process, thus leading to the reduction of the fabrication cost.

In general, a crystal silicon film has been obtained by forming an amorphous silicon film by means of plasma CVD or reduced pressure thermal CVD and then by crystallizing it by implementing a heat treatment or by irradiating laser light.

However, it has been the fact that it is difficult to obtain a required crystallinity throughout a wide area through the heat treatment because it may cause nonuniformity in the crystallization.

Further, although it is possible to obtain the high crystallinity partly by irradiating laser light, it is difficult to obtain a good annealing effect throughout the wide area. In particular, the irradiation of the laser light is apt to become unstable under the condition for obtaining the good crystallinity.

Meanwhile, a technology described in Japanese Patent Laid-Open No. Hei. 6-232059 has been known. This is a technology which allows to obtain a crystal silicon film through a heat treatment at a lower temperature than that of the prior art by introducing a metal element (e.g. nickel) which promotes the crystallization of silicon to the amorphous silicon film.

This technology allows high crystallinity to be obtained uniformly throughout a wide area as compared to the prior art crystallization method by way of only heating or crystallization of an amorphous silicon film only by means of irradiation of laser light.

However, it is difficult to obtain a crystal silicon film having high crystallinity and

homogeneity throughout a wide area which is required for an active matrix type liquid crystal display.

Further, because the metal element is contained within the film and an amount thereof to be introduced has to be controlled very carefully, there is a problem in its reproducibility and stability (electrical stability of a device obtained).

Still more, there is a problem that an elapsed change of the characteristics of a semiconductor device to be obtained is large or an OFF value, in case of a thin film transistor, is large, for example due to the influence of the remaining metal element.

That is, although the metal element which promotes the crystallization of silicon plays the useful role in obtaining the crystal silicon film, its existence becomes a minus factor which causes various problems after obtaining the crystal silicon film once.

SUMMARY OF THE INVENTION

It is an object of the invention disclosed in the present specification to provide a semiconductor device having excellent characteristics by using a crystal silicon film having a high crystallinity.

It is another object of the invention to provide a technology for reducing concentration of metal element within a crystal silicon film obtained by utilizing the metal element which promotes crystallization of silicon.

It is still another object of the present invention to provide a technology which can enhance characteristics and reliability of the semiconductor device thus obtained.

The invention disclosed in the present specification is characterized in that the metal element which promotes the crystallization of silicon is gettered by mainly utilizing fluorine. This gettering is carried out by taking the metal element into the thermal oxide film to be formed by an action of fluorine. Then, the invention is characterized in that an oxide film is formed by an action of wet oxidation at this time.

It is general to use NF_3 as means for introducing fluorine. NF_3 is a strong oxidant and promotes the formation of the thermal oxide film when it is contained in an oxidizing atmosphere in certain concentration.

However, there is a problem when NF_3 is used that etching of the surface of the silicon film advances. Especially when the metal element which promotes the crystallization of silicon is used, not a few component of metal silicide exists within the silicon film, so that there arises a problem that the component is removed concentratedly, thus roughening the surface of the silicon film and creating a gap inside.

According to the present invention disclosed in the present specification, fluorine is used just to getter the metal element. The oxide film is formed by the action of the wet oxidation by containing hydrogen within the atmosphere.

Due to the wet oxidation, the oxide film is minute and fairly flat and a film forming rate may be improved as compared to a simple thermal oxide film.

According to the present invention disclosed in the present specification, chlorine is also contained in the atmosphere in order to promote the effect of gettering the met. The

effect of eliminating the metal element from the silicon film may be enhanced by forming a compound of the metal element, fluorine and chlorine at the time of gettering by introducing chlorine.

Thus, the gettering of the metal element into the oxide film thus formed by the oxidation utilizing the action of the wet oxidation introducing hydrogen is carried out by the action of fluorine and chlorine.

Thereby, the metal element may be gettered without roughening the surface of the film or etching it locally. Then, the crystal silicon film having the high crystallinity and having low concentration of the metal element which promotes the crystallization of silicon may be obtained.

As the method for forming the oxide film to eliminate the metal element which promotes the crystallization of silicon in the present invention disclosed in the present specification, the following combinations may be cited.

Firstly, a heat treatment within an oxygen atmosphere into which 1 to 5 % of HCl and 10 ppm to 200 ppm of NF_3 are added may be cited.

Secondly, a heat treatment within an oxygen atmosphere into which 3 % of hydrogen and 50 ppm to 200 ppm of NF_3 are added may be cited.

Thirdly, a heat treatment within an oxygen atmosphere into which 3 % of hydrogen and 50 ppm to 100 ppm of ClF_3 are added may be cited.

In the heat treatments under the above-mentioned conditions, the oxide film is

formed due to the contribution that the wet oxide film is formed mainly by the action of oxygen and hydrogen. Then, the effect of gettering the metal element into the oxide film is exerted by the action of the elements such as F and Cl.

A first embodiment of the present invention is characterized in that it comprises steps of forming an amorphous silicon film; holding a metal element which promotes crystallization of silicon in contact on the surface of the amorphous silicon film; crystallizing the amorphous silicon film by implementing a first heat treatment to obtain a crystal silicon film; forming a thermal oxide film on the surface of the crystal silicon film by implementing a second heat treatment in the temperature range of 500 。C to 700。C within an atmosphere containing oxygen, hydrogen and fluorine; and eliminating the thermal oxide film.

A second embodiment of the present invention is characterized in that it comprises steps of forming an amorphous silicon film; holding a metal element which promotes crystallization of silicon in contact on the surface of the amorphous silicon film; crystallizing the amorphous silicon film by implementing a first heat treatment to obtain a crystal silicon film; forming a thermal oxide film on the surface of the crystal silicon film by implementing a second heat treatment in the temperature range of 500 。C to 700。C within an atmosphere containing oxygen, hydrogen, fluorine and chlorine; and eliminating the thermal oxide film.

A third embodiment of the present invention is characterized in that it comprises

steps of forming an amorphous silicon film; holding a metal element which promotes crystallization of silicon in contact on the surface of the amorphous silicon film; crystallizing the amorphous silicon film by implementing a heat treatment to obtain a crystal silicon film; forming a wet oxide film on the surface of the crystal silicon film within an atmosphere containing fluorine/chlorine; and eliminating the oxide film.

In the above-mentioned arrangement, the concentration of said metal element within said oxide film formed on the crystal silicon film is higher than that of said metal element within said crystal silicon film because the metal element is gettered to the oxide film.

Hydrogen added to the oxidizing atmosphere in forming the oxide film is preferable to be more than 1 % (volume %) to form the oxide film through the contribution of wet oxidation. The upper limit of the concentration is preferable to set to be below the explosion limit.

One or a plurality elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au may be used as the metal element which promotes the crystallization of silicon. It is preferable to use Ni (nickel) from its reproducibility and high effect.

The concentration of oxygen contained in the amorphous silicon film, i.e. the starting film, is preferable to be 5×10^{17} cm^{-3} to 2×10^{19} cm^{-3}. This is an important condition for obtaining the effect of gettering the metal element which promotes the crystallization of silicon.

An arrangement of fourth embodiment of the present invention is characterized in

that in a semiconductor device having a silicon film having a crystallinity, the silicon film contains a metal element which promotes crystallization of silicon in concentration of 1 x 10^{16} cm^{-3} to 5 x 10^{19} cm^{-3}, fluorine atoms in concentration of 1 x 10^{15} cm^{-3} to 1 x 10^{20} cm^{-3}, and hydrogen atoms in concentration of 1 x 10^{17} cm^{-3} to 1 x 10^{21} cm^{-3}.

The concentration of impurity and element in the present specification is defined as the minimum value of measured values measured by the SIMS (secondary ion mass spectrometry).

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of the invention and together with the description serve to explain the principle of the invention.

FIG. 1 is a diagram showing steps for obtaining a crystal silicon film;

FIG. 2 is a diagram showing steps for obtaining a crystal silicon film;

FIG. 3 is a diagram showing steps for fabricating a thin film transistor;

FIG. 4 is a diagram showing steps for fabricating a thin film transistor;

FIG. 5 is a diagram showing steps for fabricating a thin film transistor; and

FIG. 6 is a diagram showing steps for fabricating an active layer of the thin film transistor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

According to a preferred mode for carrying out the invention disclosed in the present specification, an amorphous silicon film is formed on a glass substrate at first. Then, the

amorphous silicon film is crystallized by an action of metal element typified by nickel which promotes crystallization of silicon to obtain a crystal silicon film. [0041]

This crystallization is carried out by a heat treatment in temperature of 500° C to 700° C. The metal element is contained in the crystal silicon film in the state in which the film has been crystallized by the above-mentioned heat treatment.

Next, another heat treatment is implemented within an oxidizing atmosphere containing hydrogen and NF_3. In this step, a thermal oxide film is formed mainly due to the contribution of wet oxidation and the metal element is gettered to the oxide film by the action of F (fluorine).

Next, the crystal silicon film having the high crystallinity and having low concentration of the metal element may be obtained by eliminating the thermal oxide film containing the metal element in high concentration.

Then, a thin film semiconductor device, e.g. a thin film transistor, is fabricated by using the crystal silicon film in which the concentration of the metal element is low.

Preferred Embodiment 1

The present embodiment relates to a case of obtaining a crystal silicon film on a glass substrate by utilizing nickel element.

According to the present embodiment, the crystal silicon film having a high crystallinity is obtained by the action of nickel element at first.

Then, laser light is irradiated to enhance the crystallinity of the film and to diffuse

the nickel element which is concentrated locally within the film, i.e. to reduce or to distinguish blocks of nickel.

Next, an oxide film containing F (fluorine) is formed on the crystal silicon film by thermal oxidation. At this time, the nickel element remaining in the crystal silicon film is gettered to the thermal oxide film by the action of F element. At this time, because the nickel element is dispersed therein by the irradiation of laser light, the gettering proceeds effectively.

Then, the thermal oxide film containing the nickel element in high concentration as a result of the gettering is eliminated. Thereby, the crystal silicon film in which the concentration of nickel element is low, while having the high crystallinity, is obtained on the glass substrate.

A fabrication process of the present embodiment will be explained by using FIG. 1 below. At first, a silicon oxide film 102 is formed as an underlying film in a thickness of 3000 angstrom on the glass substrate 101 of Coning 1737 (distortion point: 667。C).

The silicon oxide film formed in a thickness of 3000 angstrom by sputtering. by is used.

The silicon oxide film has a function of suppressing the diffusion of impurities from the glass substrate in the later steps. It also has a function of relaxing stress which acts between the glass substrate and a silicon film formed later.

It is also effective to include a small amount of halogen element in the underlying

film 102. Thereby, the metal element which promotes crystallization of silicon and which exists within the semiconductor layer may be gettered by the halogen element in the later step.

It is also effective to add a hydrogen plasma treatment after forming the underlying film, because it has an effect of eliminating carbonate which exists on the surface of the underlying film and of suppressing a level of fixed charge from being existing at the interface between the silicon film to be formed later.

It is also effective to implement a plasma treatment in an atmosphere in which oxygen and hydrogen are mixed as an alternate method of the hydrogen plasma treatment.

Next, an amorphous silicon film 103, which turns out to be a crystal silicon film later, is formed in a thickness of 500 angstrom by the reduced pressure thermal CVD. The reason why the reduced pressure thermal CVD is used is because thereby, the quality of the crystal silicon film obtained later is better, i.e. the film quality is denser in concrete. Beside the reduced pressure thermal CVD, the plasma CVD may be used.

The amorphous silicon film fabricated here is desirable to have 5×10^{17} cm^{-3} to 2×10^{19} cm^{-3} of concentration of oxygen within the film. It is because oxygen plays an important role in the later step of gettering the metal element (gettering of nickel in case of the present embodiment) which promotes crystallization of silicon.

However, it must be careful here because the crystallization of the amorphous silicon film is hampered if the oxygen concentration is higher than the above-mentioned

range of concentration. When the concentration of oxygen is lower than the above-mentioned concentration range on the other hand, the contribution of the metal element to the gettering effect becomes small.

The concentration of other impurities such as those of nitrogen and carbon is preferred to be low to the utmost. In concrete, the concentration is preferably below 2 x 10^{19} cm^{-3}.

The upper limit of the thickness of the amorphous silicon film is about 2000 angstrom. It is because it is disadvantageous to have a thick film to obtain the effect of laser irradiated later. Thick film is disadvantageous because the laser light irradiated to the silicon film is absorbed almost by the surface of the film.

The lower limit of the amorphous silicon film 103 is practically about 200 angstrom, though it depends on how to form it. If the thickness is below that, there will be problem in the uniformity of the film.

Next, nickel element is introduced to the amorphous silicon film 103 to crystallize it. Here, the nickel element is used as the metal element which promotes the crystallization of silicon. The nickel element is introduced by using solution.

Here, the nickel element is introduced by applying nickel acetate solution containing 10 ppm (reduced to weight) of nickel on the surface of the amorphous silicon film 103.

Beside the method of using the above-mentioned solution, sputtering, CVD, plasma treatment or adsorption may be used as the method for introducing the nickel element.

The method of using the solution is useful in that it is simple and that the concentration of the metal element may be readily adjusted.

The solution of nickel acetate salt is applied as described above to form a water film (liquid film) 104 as shown in FIG. 1A. In this state, extra solution is blown out by using a spin coater not shown. Thus, the nickel element is held in contact on the surface of the amorphous silicon film 103.

The amount of the nickel element introduced to the amorphous silicon film 103 may be controlled also by adjusting a time for holding the water film 104 and by conditions for eliminating it by using the spiner.

It is noted that it is preferable to use nickel sulfate solution for example, instead of using the nickel acetate, if the remained impurities in the later heating process is taken into consideration. It is because the nickel acetate contains carbon and it might be carbonized in the later heating process, thus remaining within the film.

Next, a heat treatment is implemented in the temperature range from 500° C to 700° C in the state shown in FIG. 1B to crystallize the amorphous silicon film 103 and to obtain a crystal silicon film 105. This heat treatment is implemented in a nitrogen atmosphere containing 3 % of hydrogen at 640° C.

It is preferable to implement the heat treatment below the temperature of the distortion point of the glass substrate. Because the distortion point of the Coning 1737 glass substrate is 667° C, the upper limit of the heating temperature here is preferable to be

about 650。C, leaving some margin.

The reason why the reducing atmosphere is adopted in the crystallization step in a way of the heat treatment is to prevent oxides from being created in the step of the heat treatment and more concretely, to suppress nickel from reacting with oxygen and NiOx from being created on the surface of the film or within the film.

Oxygen couples with nickel and contributes a lot in gettering nickel in the later gettering step. However, it has been found that if oxygen couples with nickel in the above-mentioned stage of the crystallization, it hampers the crystallization. Accordingly, it is important to suppress the oxides from being created to the utmost in the crystallization step carried out by way of heating.

The concentration of oxygen within the atmosphere for implementing the heat treatment for the crystallization has to be in an order of ppm, or preferably, less than 1 ppm.

Inert gases such as argon, beside nitrogen, may be used as the gas which occupies the most of the atmosphere for implementing the heat treatment for the crystallization.

After the crystallization step by way of the heat treatment, nickel element remains as certain blocks. This fact has been confirmed from the observation by means of TEM (transmission electron microscope).

Although the cause of the fact that the nickel exists as certain blocks is not clear yet, it is considered to be related with some crystallization mechanism.

Next, laser light is irradiated as shown in FIG. 1C. Here, KrF excimer laser

(wavelength: 248 nm) is used. Here, a method of irradiating the laser light by scanning its linear beam is adopted.

The nickel element which has been locally concentrated as a result of the crystallization carried out by way of the aforementioned heat treatment is distributed by a certain degree within the film 105 by irradiating the laser light. That is, the nickel element may be distributed by distinguishing the blocks of the nickel element.

Another heat treatment is implemented in the step shown in FIG. 1D to form a thermal oxide film for gettering the nickel element.

Here, this heat treatment is implemented within an oxygen atmosphere containing 3 % of hydrogen and 100 ppm of CLF3 at 640° C. In this step, the thermal oxide film is formed in a thickness of 200 angstrom (FIG. 1D).

This step is carried out to eliminate the nickel element which has been introduced intentionally for the crystallization in the initial stage from the crystal silicon film 105.

This heat treatment is implemented at a temperature range from 500 to 700° C. The upper limit of the heating temperature is limited by the distortion point of the glass substrate used. It must be careful not to implement the heat treatment above the distortion point of the glass substrate because, otherwise, the substrate deforms.

In this step, the nickel element which has been distributed by the above-mentioned irradiation of laser is effectively gettered to the oxide film 106.

Because the nickel element is gettered to the oxide film thus formed in the above-

mentioned step, naturally the nickel concentration within the oxide film becomes high as compared to other regions.

Further, it has been observed that the concentration of nickel element is apt to be high near the interface of the crystal silicon film 105 with the oxide film 106. It is considered to happen because the domain where the gettering mainly takes place is on the side of the oxide film near the interface between the silicon film and the oxide film. The gettering proceeding near the interface is considered to be caused by the existence of stress and defects, or organic substances near the interface.

It has been also observed that the concentration of fluorine and chlorine apt to be high near the interface between the silicon film 105 and the thermal oxide film 106.

The crystal silicon film thus formed contains the metal element which promotes crystallization of silicon in concentration of 1×10^{16} cm^{-3} to 5×10^{19} cm^{-3}, fluorine atoms in concentration of 1×10^{15} cm^{-3} to 1×10^{20} cm^{-3}, and hydrogen atoms in concentration of 1×10^{17} cm^{-3} to 1×10^{21} cm^{-3}.

After finishing to form the thermal oxide film 106 shown in FIG. 1D, the thermal oxide film 106 containing nickel in high concentration is eliminated. The thermal oxide film 106 may be eliminated by means of wet etching or dry etching using buffer hydrofluoric acid (or other hydrofluorite etchant).

Thus, a crystal silicon film 107 in which the concentration of nickel has been reduced is obtained as shown in FIG. 1E.

Because nickel element is contained near the surface of the obtained crystal silicon film 107 relatively in high concentration, it is effective to advance the above-mentioned etching to over-etch, more or less, the surface of the crystal silicon film 107.

It is also effective to irradiate laser light again after removing the thermal oxide film 106 to promote the crystallinity of the crystal silicon film 107 thus obtained further.

Although the case when the KrF excimer laser (wavelength: 248 nm) is used as the laser to be used has been shown in the present specification, it is possible to use a XeCl excimer laser (wavelength: 308 nm) and other types of excimer lasers.

It is also possible to arrange so as to irradiate ultraviolet rays or infrared rays for example instead of laser light.

Preferred Embodiment 2

The present embodiment relates to a case when Cu is used as the metal element which promotes the crystallization of silicon in the arrangement shown in the first embodiment. In this case, cupric acetate [$Cu(CH_3COO)_2$] or cupricchloride ($CuCl_2 2H_2O$) may be used as the solution for introducing Cu.

Preferred Embodiment 3

The present embodiment relates to a case of growing crystal in the form different from that in the first embodiment. That is, the present embodiment relates to a method of growing the crystal in a direction parallel to the substrate, i.e. a method called lateral growth, by utilizing the metal element which promotes crystallization of silicon. [0096]

FIG. 2 shows the fabrication process according to the present embodiment. At first, a silicon oxide film is formed as an underlying film 202 in a thickness of 3000 angstrom on the Coning 1737 glass substrate (or a quartz substrate) 201.

Next, an amorphous silicon film 203 which is the starting film of a crystal silicon film is formed in a thickness of 600 angstrom by reduced pressure thermal CVD. The thickness of the amorphous silicon film is preferable to be less than 2000 angstrom as described before.

Next, a silicon oxide film not shown is formed in a thickness of 1500 angstrom and is patterned to form a mask 204. An opening is created on the mask in a domain 205. The amorphous silicon film 203 is exposed at the domain where the opening 205 is created.

The opening 205 has a thin and long rectangular shape in the longitudinal direction from the depth to the front side of the figure. Preferably, the width of the opening 203 is 20 μm or more. The length thereof in the longitudinal direction may be determined arbitrarily.

Then, the nickel acetate aqueous solution containing 10 ppm of nickel element in terms of weight is applied in the same manner with the first embodiment and the extra solution is removed by implementing spin drying by using a spinner not shown.

Thus, the solution is held in contact on the exposed surface of the amorphous silicon film 203 as indicated by a dot line 206 in FIG. 2A.

Next, a heat treatment is implemented at 640° C for four hours in a nitrogen

atmosphere containing 3 % of hydrogen and in which oxygen is minimized. Then, crystal grows in the direction parallel to the substrate as indicated by the reference numeral 207 in FIG. 2B. This crystal growth advances from the domain of the opening 205 to which nickel element has been introduced to the surrounding part. This crystal growth in the direction parallel to the substrate will be referred to as lateral growth.

It is possible to advance this lateral growth across more than 100 μm under the conditions shown in the present embodiment. Then, a silicon film 208 having the domain in which the crystal has thus grown laterally is obtained. It is noted that crystal growth in the vertical direction called vertical growth advances from the surface of the silicon film to the underlying interface in the domain where the opening 205 is formed.

Then, the mask 204 made of the silicon oxide film for selectively introducing nickel element is eliminated. Thus, the state shown in FIG. 2C is obtained. In this state, the vertically grown domain, the laterally grown domain and a domain in which no crystal has grown (having amorphous state) exist within the silicon film 208.

In this state, the nickel element is unevenly distributed in the film. In particular, the nickel element exists relatively in high concentration at the domain where the aperture 205 has been formed and at the edge portion 207 of the crystal growth.

After obtaining the state shown in FIG. 2C, laser light is irradiated. The KrF excimer laser is irradiated here similarly to the first embodiment.

The nickel element which has been unevenly distributed is diffused in this step to

obtain a condition in which it can be gettered readily in the later gettering step.

After irradiating the laser light, a heat treatment is implemented at 650。C for 12 hours within an atmosphere of containing 3 % of hydrogen and 100 ppm of NF_3. In this step, an oxide film 209 containing nickel element in high concentration is formed in a thickness of 200 angstrom. In the same time, the concentration of nickel element within the silicon film 208 may be reduced relatively (FIG. 2D).

After finishing to form the thermal oxide film by the above-mentioned heat treatment, the thermal oxide film 209 containing nickel element in high concentration is eliminated.

It is useful to etch the surface of the crystal silicon film after eliminating the thermal oxide film 209.

Next, patterning is implemented to form a pattern 210 formed of the laterally grown domain.

The concentration of nickel element which remains within the pattern 210 made of the laterally grown domain thus obtained may be reduced further as compared to the case shown in the first embodiment.

This is caused by the fact that the concentration of the metal element contained within the laterally grown domain is low originally. In concrete, the concentration of nickel element within the pattern 209 made of the laterally grown domain may be readily reduced to the order of 10^{17} cm^{-3} or less.

It is noted that it is useful to implement the etching process further after forming the pattern shown in FIG. 2E to eliminate the nickel element existing on the surface of the pattern.

Then, a thermal oxide film 211 is formed after thus forming the pattern 210. This thermal oxide film is formed into a thickness of 200 angstrom by implementing a heat treatment for 12 hours in an oxygen atmosphere at 650。C.

It is also effective to include fluorine within the atmosphere in forming the thermal oxide film 211. If fluorine is included in the atmosphere in forming the thermal oxide film 211, the nickel element may be fixed and unpaired bonding hands on the surface of the silicon film may be neutralized. That is, the interfacial characteristics between the active layer and the gate insulating film may be improved.

Chlorine may be used instead of Fluorine.

It is noted that the thermal oxide film becomes a part of the gate insulating film later when a thin film transistor is formed.

If the thin film transistor is to be fabricated thereafter, a silicon oxide film is formed further by means of plasma CVD or the like so as to cover the thermal oxide film 211 to form a gate insulating film.

Preferred Embodiment 4

The present embodiment relates to a case of fabricating a thin film transistor disposed in a pixel domain of an active matrix type liquid crystal display or an active matrix

type EL display by utilizing the invention disclosed in the present specification.

FIG. 3 shows the fabrication process according to the present embodiment. At first, the crystal silicon film is formed on the glass substrate through the process shown in the first or the third embodiment. When the crystal silicon film is obtained by the arrangement shown in the first embodiment, it is patterned to obtain the state shown in FIG. 3A.

In the state shown in FIG. 3A, the reference numeral (301) denotes a glass substrate, (302) an underlying film, and (303) an active layer formed of the crystal silicon film. After obtaining the state shown in FIG. 3A, a plasma treatment is implemented within a reduced pressure atmosphere in which oxygen and hydrogen are mixed. The plasma is generated by high-frequency discharge.

Organic substances existing on the surface of the exposed active layer 303 may be removed by the above-mentioned plasma treatment. Specifically, the organic substances adsorbing on the surface of the active layer are oxidized by oxygen plasma and the oxidized organic substances are reduced and vaporized further by hydrogen plasma. Thus the organic substances existing on the surface of the exposed active layer 303 are removed.

The removal of the organic substances is very effective in suppressing fixed charge from existing on the surface of the active layer 303. Because the fixed charge caused by the existence of organic substances hampers the operation of the device and renders the characteristics thereof instable, it is very useful to reduce it.

After removing the organic substances, thermal oxidation is implemented within an

oxygen atmosphere at 640° C to form a thermal oxide film 300 of 100 angstrom thick. This thermal oxide film has a high interfacial characteristic with a semiconductor layer and composes a part of a gate insulating film later. Thus, the state shown in FIG. 3A is obtained.

After obtaining the state shown in FIG. 3A, a silicon oxide film 304 which composes the gate insulating film is formed in a thickness of 1000 angstrom. The film may be formed by using plasma CVD (FIG. 3B).

The silicon oxide film 304 functions as the gate insulating film together with the thermal oxide film 300.

It is also effective to contain halogen element within the silicon oxide film 304. In this case, the nickel element may be fixed by the action of the halogen element. Then, it is possible to suppress the function of the gate insulating film as an insulating film from dropping by the influence of the nickel element (or another metal element which promotes crystallization of silicon) existing within the active layer.

After forming the silicon oxide film 304 which functions as the gate insulating film, an aluminum film not shown which functions as a gate electrode later is formed by sputtering. 0.2 weight % of scandium is included within the aluminum film.

Scandium is included in the aluminum film to suppress hillock and whisker from being produced in the later process. The hillock and whisker mean that abnormal growth of aluminum occurs by heating, thus forming needle or prickle-like projections.

After forming the aluminum film, a dense anodic oxide film not shown is formed. The anodic oxide film is formed by using ethylene glycol solution containing 3 % of tartaric acid as electrolyte by setting the aluminum film as the anode and platinum as the cathode. The thickness of the anodic oxide film having the dense film quality is around 100 angstrom.

This anodic oxide film plays a role of enhancing the adhesiveness with a resist mask to be formed later.

The thickness of the anodic oxide film may be controlled by adjusting voltage applied during the anodization.

Next, the resist mask 306 is formed and the aluminum film is patterned so as to have a pattern 305. The state shown in FIG. 3B is thus obtained.

Here, another anodization is implemented. In this case, 3 % of oxalate aqueous solution is used as electrolyte. A porous anodic oxide film 308 is formed by anodizing within this electrolyte by setting the aluminum pattern 305 as the anode.

In this step, the anodic oxide film 308 is formed selectively on the sides of the aluminum pattern because the resist mask 306 having the high adhesiveness exists thereabove.

The anodic oxide film may be grown up to several μm thick. The thickness is 6000 angstrom here. It is noted that the range of the growth may be controlled by adjusting an anodizing time.

Next, the resist mask 306 is removed. Then, a dense anodic oxide film is formed again. That is, the anodization is implemented again by using the ethylene glycol solution containing 3 % of tartaric acid as electrolyte.

Then, an anodic oxide film 309 having a dense film quality is formed because the electrolyte infiltrates into the porous anodic oxide film 308.

This dense anodic oxide film 309 is 1000 angstrom thick. The thickness is controlled by adjusting applied voltage.

Here, the exposed silicon oxide film 304 and the thermal oxide film 300 are etched by utilizing dry etching. Then, the porous anodic oxide film 308 is eliminated by using mixed acid in which acetic acid, nitric acid and phosphoric acid are mixed. Thus, the state shown in FIG. 3D is obtained.

After obtaining the state shown in FIG. 3D, impurity ions are injected. Here, P (phosphorus) ions are injected by plasma doping in order to fabricate an N-channel type thin film transistor.

In this step, heavily doped domains 311 and 315 and lightly doped domains 312 and 314 are formed because part of the remaining silicon oxide film 310 functions as a semi-permeable mask, thus blocking part of the injected ions.

Then, laser light or intense light is irradiated to activate the domains into which the impurity ions have been injected. Thus, a source domain 311, a channel forming domain 313, a drain domain 315 and low concentrate impurity domains 312 and 314 are formed in

a manner of self-adjustment.

One designated by the reference numeral 314 here is the domain called the LDD (lightly doped domain) (FIG. 3D).

It is noted that when the dense anodic oxide film 309 is formed as thick as 2000 angstrom or more, an offset gate domain may be formed on the outside of the channel forming domain 313 by its thickness.

Although the offset gate domain is formed also in the present embodiment, it is not shown in the figures because its size is small, its contribution due to the existence thereof is small and the figures might otherwise become complicated.

It must be careful to form the anodic oxide film having the dense quality as thick as 2000 angstrom or more because it requires more than 200 V of applied voltage.

Next, a silicon oxide film or a silicon nitride film or their laminated film is formed as an interlayer insulating film 316. The interlayer insulating film may be constructed by forming a layer made of a resin material on the silicon oxide film or the silicon nitride film.

Then, contact holes are created to form a source electrode 317 and a drain electrode 318. Thus, the thin film transistor shown in FIG. 3E is completed.

Preferred Embodiment 5

The present embodiment relates to a case of fabricating a thin film transistor through a process different from that shown in FIG. 3.

FIG. 4 shows the fabrication process according to the present embodiment. At first,

the crystal silicon film is formed on the glass substrate through the process shown in the first or third embodiment. It is then patterned, thus obtaining the state shown in FIG. 4A.

After obtaining the state shown in FIG. 4A, a plasma treatment is implemented within a reduced pressure atmosphere in which oxygen and hydrogen are mixed.

In the state shown in FIG. 4A, the reference numeral (401) denotes a glass substrate, (402) an underlying film, (403) an active layer made of the crystal silicon film and (400) a thermal oxide film formed again after eliminating the thermal oxide film for gettering.

After obtaining the state shown in FIG. 4A, a silicon oxide nitride film 404 which composes a gate insulating film is formed in a thickness of 1000 angstrom (FIG. 4B).

The silicon oxide nitride film 404 composes the gate insulating film together with the thermal oxide film 400.

Next, an aluminum film not shown which functions as a gate electrode later is formed by sputtering. 0.2 weight % of scandium is included within the aluminum film.

After forming the aluminum film, a dense anodic oxide film not shown is formed. The anodic oxide film is formed by using ethylene glycol solution containing 3 % of tartaric acid as electrolyte.

[0159]

The thickness of the anodic oxide film not shown having the dense film quality is around 100 angstrom. This anodic oxide film plays a role of enhancing the adhesiveness with a resist mask to be formed later.

It is noted that the thickness of the anodic oxide film may be controlled by adjusting voltage applied during the anodization.

Next, the resist mask 405 is formed and the aluminum film is patterned so as to have a pattern 406.

Here, another anodization is implemented. In this case, 3 % of oxalate aqueous solution is used as electrolyte. A porous anodic oxide film 407 is formed by anodizing within this electrolyte by setting the aluminum pattern 406 as the anode.

In this step, the anodic oxide film 407 is formed selectively on the sides of the aluminum pattern because the resist mask 405 having the high adhesiveness exists thereabove.

The anodic oxide film may be grown up to several μm thick. The thickness is 6000 angstrom here. It is noted that the range of the growth may be controlled by adjusting an anodizing time.

Then, the resist mask 405 is removed and another dense anodic oxide film is formed. That is, the anodization is implemented again by using the ethylene glycol solution containing 3 % of tartaric acid as electrolyte. Then, an anodic oxide film 408 having a dense film quality is formed because the electrolyte infiltrates into the porous anodic oxide film 407 (FIG. 2C).

Here, the initial injection of impurity ions is implemented. Here, P ions are injected to fabricate an N-channel type thin film transistor. If a P-channel type thin film transistor

is to be fabricated, B (boron) ions are injected.

A source domain 409 and a drain domain 411 are formed by injecting the impurity ions. No impurity ion is injected to a domain 410.

Then, the porous anodic oxide film 407 is eliminated by using mixed acid in which acetic acid, nitric acid and phosphoric acid are mixed. Thus, the state shown in FIG. 4D is obtained.

After obtaining the state shown in FIG. 4D, impurity ions (phosphorus ions) are injected again. The impurity ions are injected under the doping condition lighter (lower dosage) than that of the first injection.

In this step, lightly doped domains 412 and 413 are formed and a domain 414 turns out to be a channel forming domain (FIG. 4D).

Then, laser light or intense light is irradiated to activate the domains into which the impurity ions have been injected. Thus, the source domain 409, the channel forming domain 414, the drain domain 411 and low concentrate impurity domains 412 and 413 are formed in a manner of self-adjustment.

Here, one designated by the reference numeral 413 is the domain called the LDD (lightly doped domain) (FIG. 4D).

Next, a silicon oxide film or a silicon nitride film or their laminated film is formed as an interlayer insulating film 414. The interlayer insulating film may be constructed by forming a layer made from a resin material on the silicon oxide film or the silicon nitride

film.

Then, contact holes are created to form a source electrode 416 and a drain electrode 417. Finally, a heat treatment of an hour is implemented within a hydrogen atmosphere at 350。C (hydrogen heat treatment). In this step, the defects and unpaired coupling hands within the active layer is neutralized. Thus, the thin film transistor shown in FIG. 4E is completed.

Preferred Embodiment 6

The present embodiment relates to a case when an N-channel type thin film transistor and a P-channel type thin film transistor are formed in a complementary manner.

The arrangement shown in the present embodiment may be utilized for various thin film integrated circuits integrated on an insulated surface as well as for peripheral driving circuits of an active matrix type liquid crystal display for example.

At first, a silicon oxide film or a silicon oxide nitride film is formed as an underlying film 502 on a glass substrate 501 as shown in FIG. 5A.

Next, an amorphous silicon film not shown is formed by the plasma CVD or reduced pressure thermal CVD. Then, the amorphous silicon film is transformed into a crystal silicon film by the same method as shown in the first embodiment.

Next, a plasma treatment is implemented within an atmosphere in which oxygen and hydrogen are mixed. Then, the obtained crystal silicon film is patterned to obtain active layers 503 and 504. After forming the active layers 503 and 504, a thermal oxide film 500

is formed. This thickness of the thermal oxide film 500 is set at about 100 angstrom.

Thus, the state shown in FIG. 5A is obtained. Next, a silicon oxide film 505 which compose the gate insulating film is formed. Then, an aluminum film not shown which composes a gate electrode later is formed in a thickness of 4000 angstrom by sputtering. Beside the aluminum film, a metal which can be anodized (e.g. tantalum) may be used.

After forming the aluminum film, a very thin and dense anodic oxide film not shown is formed on the surface thereof by the method described before.

Next, a resist mask not shown is placed on the aluminum film to pattern the aluminum film. Then, anodization is implemented by setting the obtained aluminum pattern as the anode to form porous anodic oxide films 508 and 509. The thickness of the porous anodic oxide films is 5000 angstrom for example.

Then, the resist mask not shown is removed and another anodization is implemented under the condition of forming dense anodic oxide films to form dense anodic films 510 and 511. The thickness of the dense anodic oxide films 510 and 511 is 800 angstrom. Thus, the state shown in FIG. 5B is obtained.

Then, the exposed silicon oxide film 505 and the thermal oxide film 500 are eliminated by dry etching, thus obtaining the state shown in FIG. 5C.

After obtaining the state shown in FIG. 5C, the porous anodic oxide films 508 and 509 are eliminated by using mixed acid in which acetic acid, nitric acid and phosphoric acid are mixed. Thus, the state shown in FIG. 5D is obtained.

Here, resist masks are disposed alternately to inject P ions to the thin film transistor on the left side and B ions to the thin film transistor on the right side.

By injecting those impurity ions, a source domain 514 and a drain domain 517 having N-type in high concentration are formed in a manner of self-adjustment.

Further, a domain 515 to which P ions are doped in low concentration, thus having weak N-type, as well as a channel forming domain 516 are formed in the same time.

The reason why the domain 515 having the weak N-type is formed is because the remaining gate insulating film 512 exists. That is, part of P ions transmitting through the gate insulating film 512 is blocked by the gate insulating film 512.

By the same principle, a source domain 521 and a drain domain 518 having strong P-type are formed in a manner of self-adjustment and a low concentrate impurity domain 520 is formed in the same time. Further, a channel forming domain 519 is formed in the same time.

It is noted that when the thickness of the dense anodic oxide films 510 and 511 is as thick as 2000 angstrom, an offset gate domain may be formed in contact with the channel forming domain by that thickness.

Its existence may be ignored in the case of the present embodiment because the dense anodic oxide films 510 and 511 are so thin as less than 1000 angstrom.

Then, laser light or intense light is irradiated to anneal the domain into which the impurity ions have been injected.

Then, a silicon nitride film 522 and a silicon oxide film 523 are formed as interlayer insulating films as shown in FIG. 5E. Their thickness is 1000 angstrom, respectively. It is noted that the silicon oxide film 523 needs not be formed.

Here, the thin film transistor is covered by the silicon nitride film. The reliability of the thin film transistor may be enhanced by arranging as described above because the silicon nitride film is dense and has a favorite interfacial characteristic.

Further, an interlayer insulating film 524 made of a resin material is formed by means of spin coating. Here, the thickness of the interlayer insulating film 524 is 1 μm (FIG. 5E).

Then, contact holes are created to form a source electrode 525 and a drain electrode 526 of the N-channel type thin film transistor on the left side. In the same time, a source electrode 527 and the drain electrode 526 of the thin film transistor on the right side are formed. Here, the electrode 526 is disposed in common.

Thus, the thin film transistor circuit having a CMOS structure constructed in a complementary manner may be formed.

According to the arrangement shown in the present embodiment, the thin film transistor is covered by the nitride film as well as the resin material. This arrangement allows to enhance the durability of the thin film transistor to which movable ions nor moisture hardly infiltrate.

Further, it allows to prevent capacitance from being generated between the thin film

transistor and wires when a multi-layered wire is formed.

Preferred Embodiment 7

The present embodiment relates to a case when nickel element is introduced directly to the surface of the underlying film in the process shown in the first embodiment. In this case, the nickel element is held in contact with the lower surface of the amorphous silicon film.

In this case, nickel element is introduced after forming the underlying film such that the nickel element (metal element) is held in contact with the surface of the underlying film. Beside the method of using the solution, sputtering, CVD or adsorption may be used as the method for introducing nickel element.

Preferred Embodiment 8

The present embodiment is characterized in that the crystallinity of an island pattern formed of a crystal silicon film obtained by irradiating laser light in the state shown in FIG. 2E, the state shown in FIG. 3A or the state shown in FIG. 4A is improved.

A predetermined annealing effect can be obtained with relatively low irradiation energy density by irradiating the laser light in the state shown in FIGs. 2E, 3A and 4A.

It is considered to have been effected because the laser energy is irradiated to a spot of small area, thus enhancing the efficiency of energy utilized in the annealing.

Preferred Embodiment 9

The present embodiment relates to a case of fabricating a bottom-gate type thin film

transistor. FIG. 6 shows the process for fabricating the thin film transistor of the present embodiment. At first, a silicon oxide film 602 is formed as an underlying film on a glass substrate 601.

Next, a gate electrode 608 is formed by using an adequate metallic material or metallic sillicide material (FIG. 6A).

After forming the gate electrode 603, a silicon oxide film 604 which functions as a gate insulating film is formed. Further, an amorphous silicon film 605 is formed.

After forming the amorphous silicon film 605, nickel acetate aqueous solution is applied so that nickel element is held in contact on the surface of the amorphous silicon film 605 as indicated by numeral 607 (FIG. 6B).

Next, a heat treatment is implemented within an nitrogen atmosphere containing 3 % of hydrogen at 650。C to crystallize the amorphous silicon film 605 and to obtain a crystal silicon film 606.

After forming the amorphous silicon film, a heat treatment is implemented within an oxygen atmosphere containing 5 % of HCl and 100 ppm (volume) of NF_3 at 650。C. A thermal oxide film 609 is formed in this heat treatment (FIG. 6C).

Then, the thermal oxide film 609 is eliminated.

Next, the crystal silicon film 606 and the gate insulating film 604 are patterned to form an active layer 612 of the thin film transistor. Further, a resist mask 610 is placed (FIG. 6D).

In the state shown in FIG. 6D, impurity ions are injected to form source and drain domains. Here, P (phosphorus) ions are injected in order to fabricate a N-channel type thin film transistor. In this step, the source domain 613 and the drain domain 614 are formed.

After that, isotropic ashing is implemented to cause the resist mask 610 to recede as a whole. That is, the size of the resist mask 610 is reduced as a whole. Thus, the receded resist mask 615 is obtained (FIG. 6E).

Then, P ions are injected again in the state shown in FIG. 6E. This step is implemented with less dosage than the dosage of P ions in the step in FIG. 6D. Thus, low concentrate impurity domains 616 and 617 are formed.

Next, metallic electrodes 618 and 619 are formed. Here, the electrode 618 is the source electrode and the electrode 619 is the drain electrode. Thus, the bottom-gate type thin film transistor is completed.

The use of the invention disclosed in the present specification allows to provide the technology for reducing the concentration of metal element within the crystal silicon film which has been obtained by utilizing the metal element which promotes the crystallization of silicon.

The use of this technology also allows a more reliable and higher performance thin film semiconductor device to be obtained.

[Document Name] Specification

[Title of the Invention] A Method Of Manufacturing A Semiconductor Device

[Claims]

1. A method for fabricating a semiconductor device, comprising steps of:

forming an amorphous silicon film;

contacting and holding a metal element which promotes crystallization of silicon on the surface of said amorphous silicon film;

crystallizing said amorphous silicon film by implementing a first heat treatment to obtain a crystal silicon film;

forming a thermal oxide film on the surface of said crystal silicon film by implementing a second heat treatment in the temperature range of 500°C to 700°C within an atmosphere containing oxygen, hydrogen and fluorine; and

removing said thermal oxide film.

METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

ABSTRACT

A first heat treatment for crystallization is implemented after introducing nickel to an amorphous silicon film 103 disposed on a quartz substrate 101. A crystal silicon film 105 is obtained by this heat treatment. Then, a oxide film 106 is formed by wet oxidation. At this time, the nickel element is gettered to the oxide film 106 by an action of fluorite. Then, the oxide film 106 is removed. Thereby, a crystal silicon film 107 having low concentration of the metal element and a high crystallinity can be obtained.

FIG. 1A

FORMATION OF AMORPHOUS SILICON FILM AND INTRODUCTION OF N1 ELEMENT

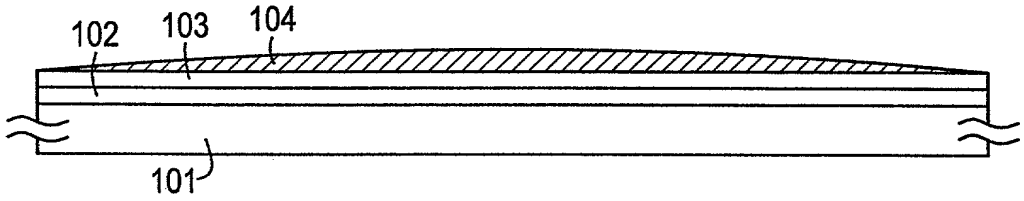


FIG. 1B

HEAT TREATMENT FOR CRYSTALLIZATION

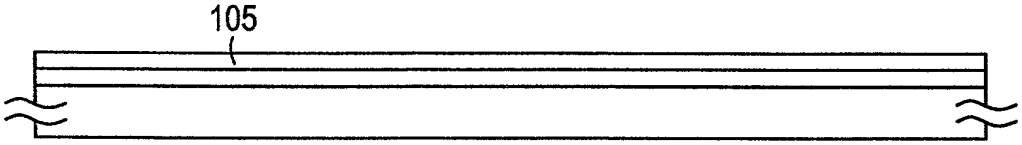


FIG. 1C

IRRADIATION OF LASER LIGHT

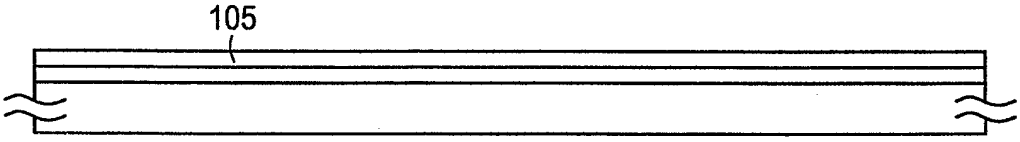


FIG. 1D

FORMATION OF WET OXIDE FILM CONTAINING FLUORITE

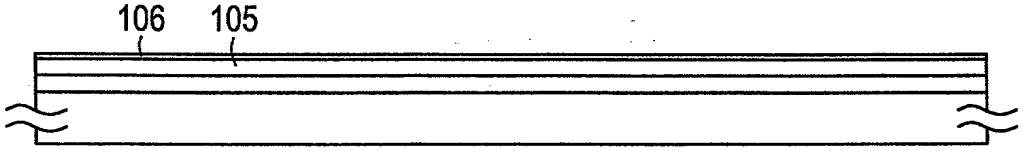


FIG. 1E

REMOVAL OF OXIDE FILM CONTAINING NI

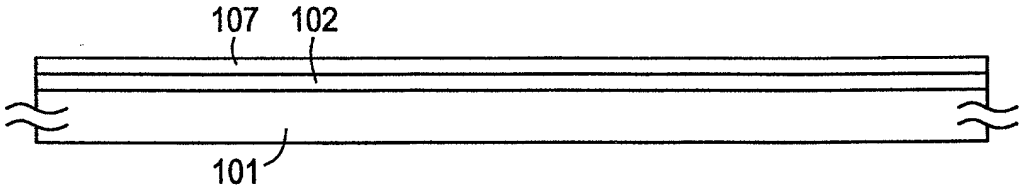


FIG. 2A

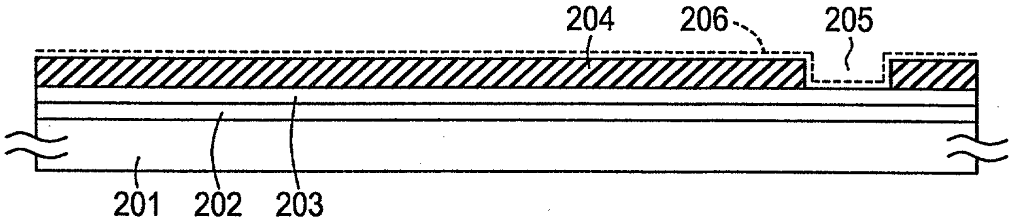


FIG. 2B

HEAT TREATMENT FOR CRYSTALLIZATION

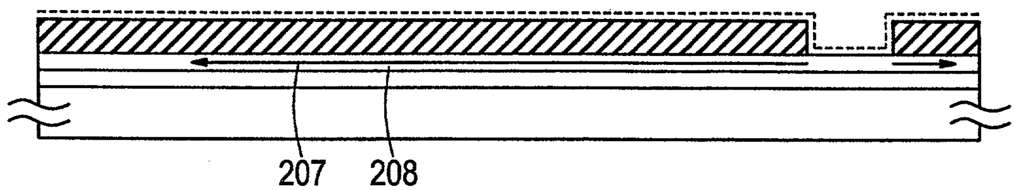


FIG. 2C

IRRADIATION OF LASER LIGHT

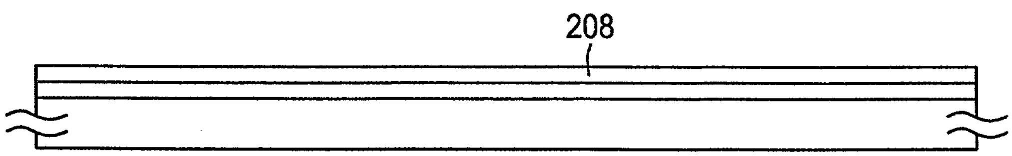


FIG. 2D

FORMATION OF WET OXIDE FILM
CONTAINING FLUORITE

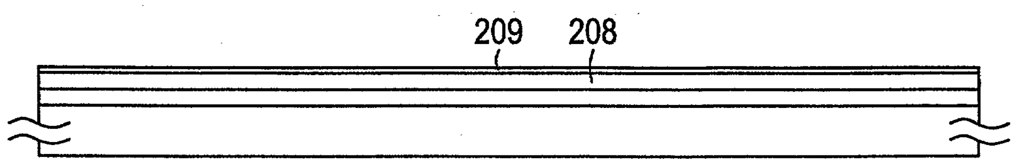


FIG. 2E

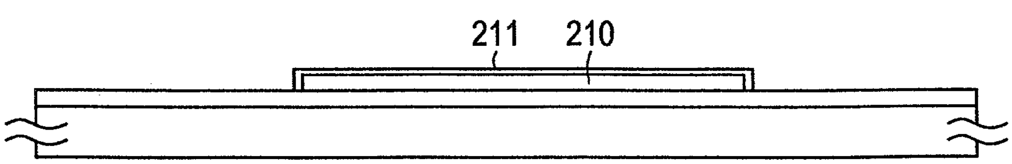


FIG. 3A

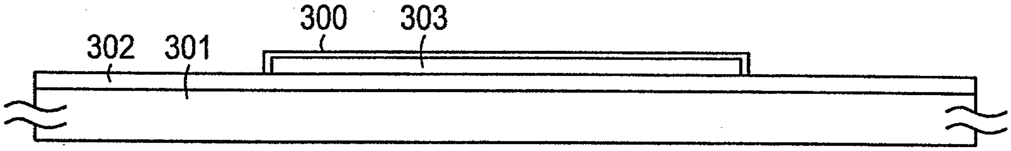


FIG. 3B

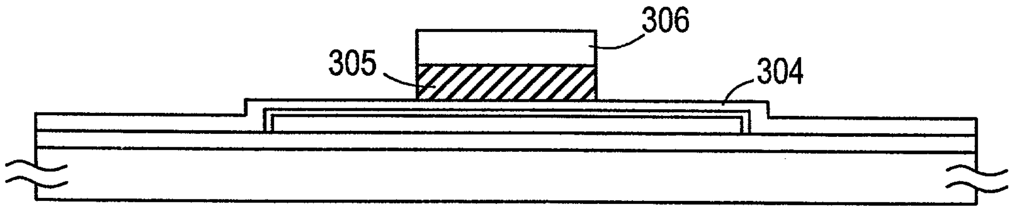


FIG. 3C

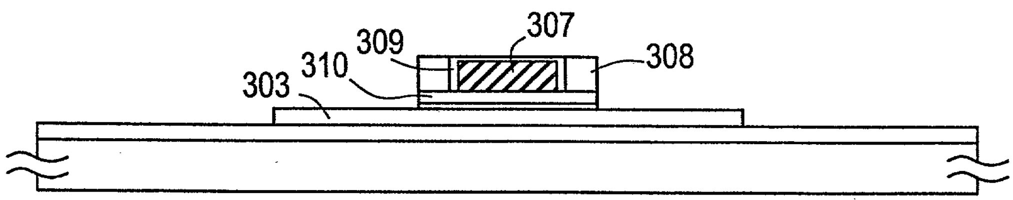


FIG. 3D

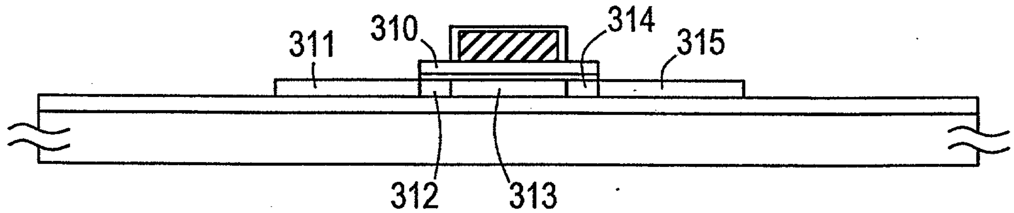


FIG. 3E

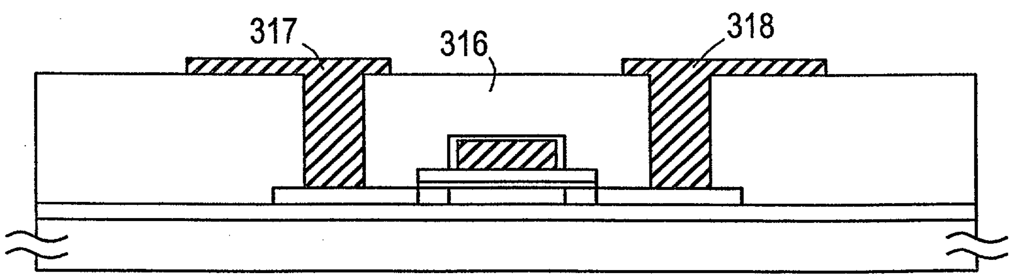


FIG. 4A

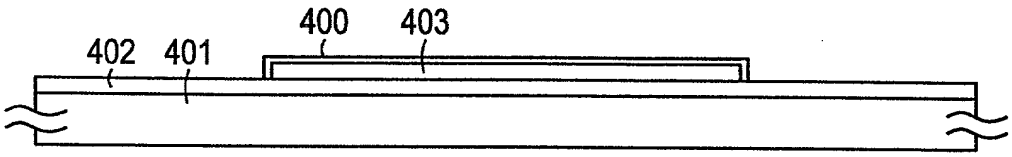


FIG. 4B

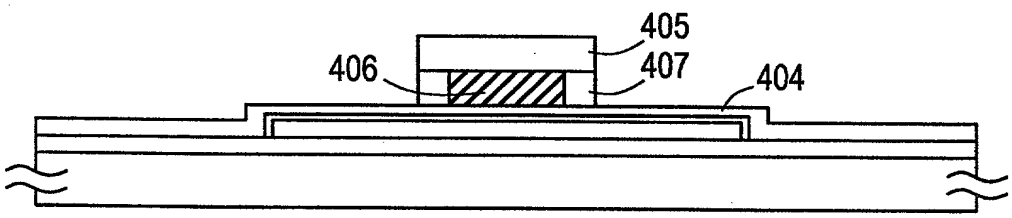


FIG. 4C

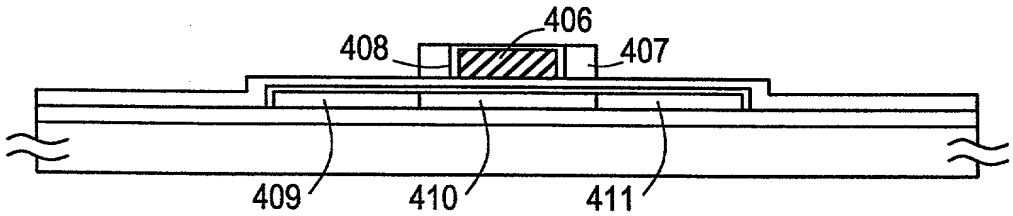


FIG. 4D

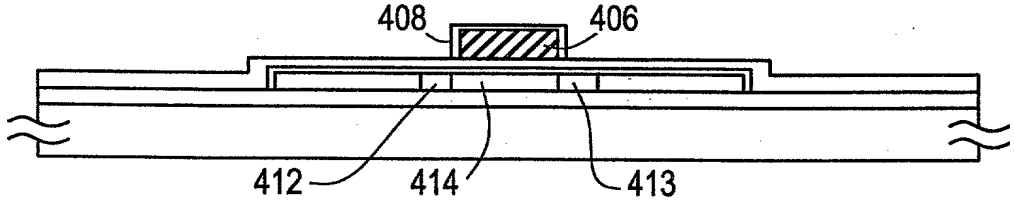


FIG. 4E

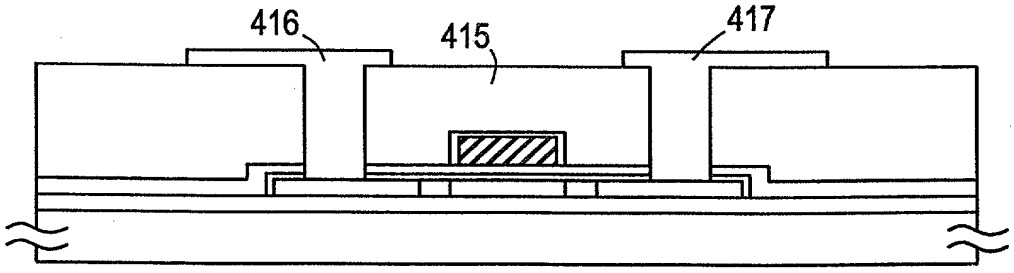


FIG. 5A

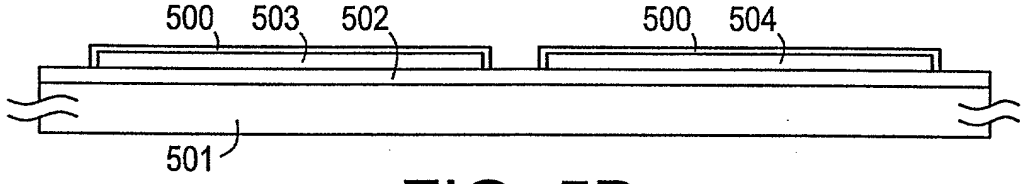


FIG. 5B

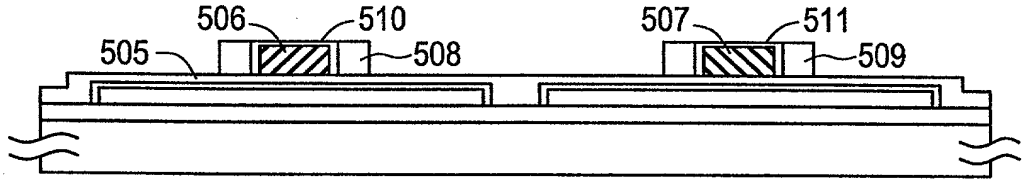


FIG. 5C

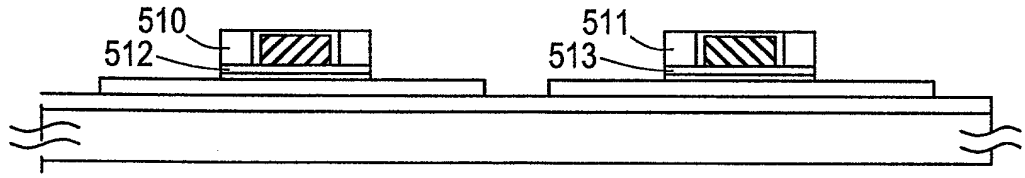


FIG. 5D

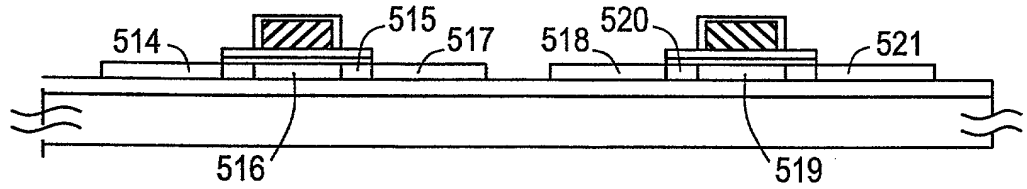


FIG. 5E

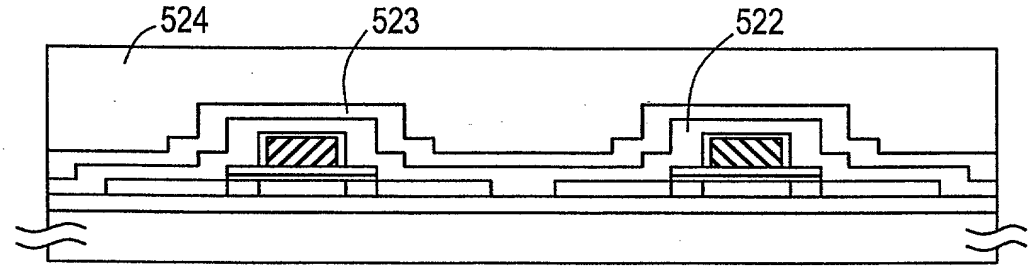


FIG. 5F

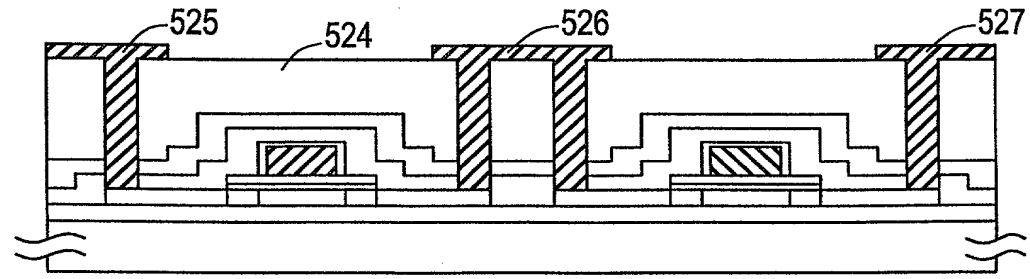


FIG. 6A

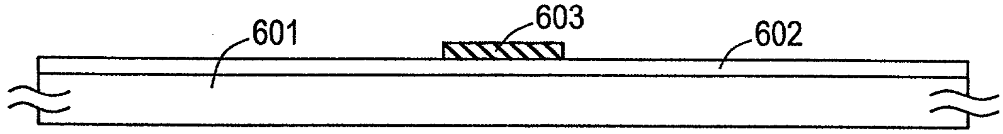


FIG. 6B

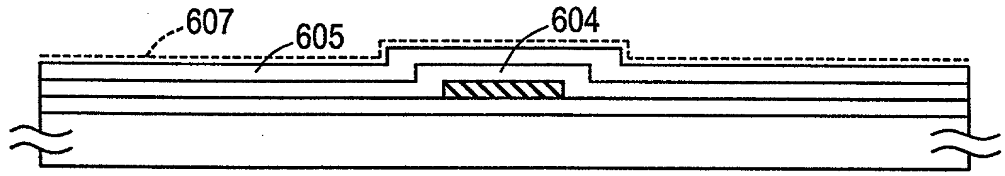


FIG. 6C

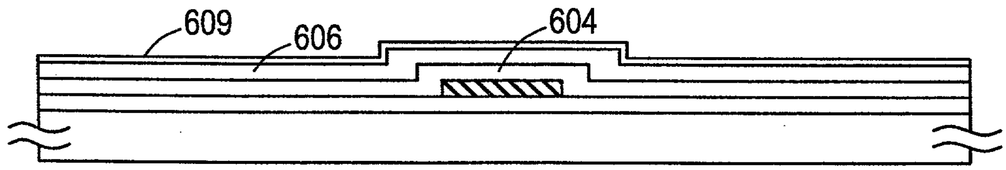


FIG. 6D

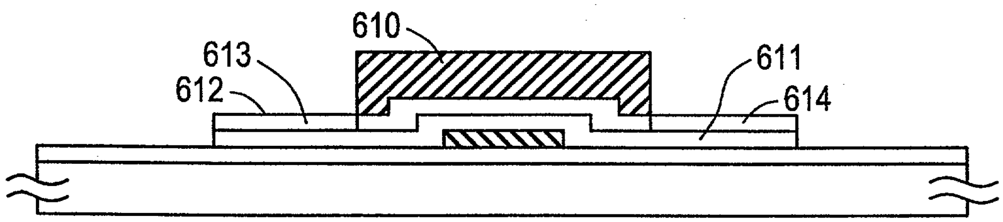


FIG. 6E

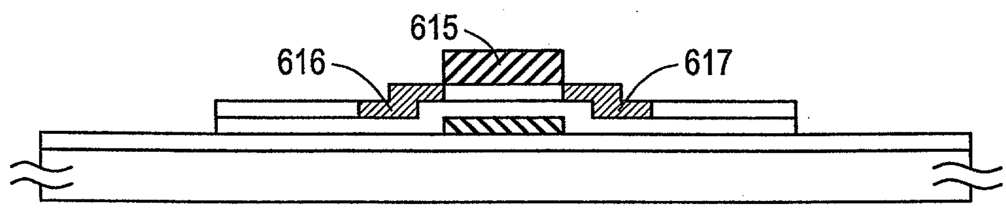
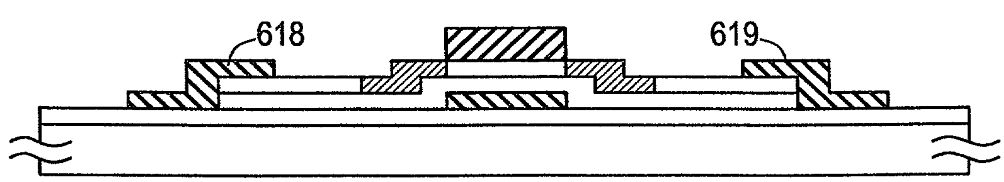


FIG. 6F



DECLARATION AND POWER OF ATTORNEY FOR **PATENT APPLICATION**

ATTORNEY DOCKET NO.
0756-1610

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: * A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

, the specification of which is attached hereto unless the following box is checked:

Insert Title

Check Box If Appropriate — For Use Without Specification Attached

☒ The specification was filed on January 16, 1997
and was assigned Serial No. 08/784,294 (if known)
and was amended on (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s)

Priority Claimed

Insert Priority Information (if appropriate)

(Number)	(Country)	(Month/Day/Year Filed)	Yes	No
8-88759	JAPAN	March 17, 1996	☒	☐
			☐	☐
			☐	☐
			☐	☐
			☐	☐
			☐	☐

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status—patented, pending, abandoned)

Revised 11/90

*NOTE: Must be completed.

I hereby appoint the following attorneys to prosecute this application and/or an international application and to transact all business in the Patent and Trademark Office connected therewith:

Daniel W. Sixbey (Reg. No. 20,932)
Stuart J. Friedman (Reg. No. 24,312)
Charles M. Leedom, Jr. (Reg. No. 26,477)
Gerald J. Ferguson, Jr. (Reg. No. 23,016)
David S. Safran (Reg. No. 27,997)
Thomas W. Cole (Reg. No. 28,290)

Send Correspondence to:

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
2010 Corporate Ridge, Suite 600
McLean, Virginia 22102
Telephone: (703) 790-9110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Insert Name of Non-U.S. firm, attorney or agent

The undersigned hereby authorize any U. S. attorney or agent named herein to accept and follow instructions from _____ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

Insert Full Name of First or Sole Inventor and Date This Document Is Signed

FULL NAME OF SOLE OR FIRST INVENTOR	INVENTOR'S SIGNATURE	DATE
Shunpei YAMAZAKI	Shunpei Yamazaki	04/25/1997
RESIDENCE (City, State & Country)		CITIZENSHIP
Tokyo, Japan		Japanese
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		
4-10-20, Seijo, Setagaya-ku, Tokyo 157 Japan		

Insert Residence
Insert Citizenship
Insert Post Office Address

Second Inventor: see above	FULL NAME OF SECOND JOINT INVENTOR, IF ANY	INVENTOR'S SIGNATURE	DATE
	Hisashi OHTANI	Hisashi Ohtani	05/07/1997
	RESIDENCE (City, State & Country)		CITIZENSHIP
	Kanagawa, Japan		Japanese
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		
	Mac Aikoishida Court 501, 7-896-1, Takamori, Isehara-shi, Kanagawa-ken 259-11 Japa		

Third Inventor: see above	FULL NAME OF THIRD JOINT INVENTOR, IF ANY	INVENTOR'S SIGNATURE	DATE
	Toshiji HAMATANI	Toshiji Hamatani	05/07/1997
	RESIDENCE (City, State & Country)		CITIZENSHIP
	Kanagawa, Japan		Japanese
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		
	987-4, Hase, Atsugi-shi, Kanagawa-ken 243 Japan		

Fourth Inventor: see above	FULL NAME OF FOURTH JOINT INVENTOR, IF ANY	INVENTOR'S SIGNATURE	DATE
	RESIDENCE (City, State & Country)		CITIZENSHIP
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		

Docket No. 0756-2131

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of	)
Shunpei YAMAZAKI et al.	)
Based On Serial No. 08/784,294	) Art Unit: 2811
Which Was Filed: January 16, 1997	) Examiner: F. Abraham
For: A METHOD OF MANUFACTURING	)
A SEMICONDUCTOR DEVICE	) Date: March 24, 2000

NOTICE OF CHANGE OF ADDRESS

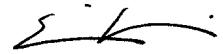
Honorable Assistant Commissioner for Patents
Washington, D.C. 20231
Sir:

Effective immediately, please note that the address of the attorney(s) of record in the above-referenced application has been changed. Please direct all future correspondence to:

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102

Telephone (703) 790-9110

Respectfully submitted,



Eric J. Robinson
Registration No. 38,285

Nixon Peabody LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110